## Specification Amendments

Please replace the title of the invention, which appears on page 1, line 1, with the following new title:

A METHOD OF FABRICATING COMPLEMENTARY HIGH-VOLTAGE FIELD-EFFECT TRANSISTORS

Please replace the Abstract of the Disclosure with the following new abstract, which is also being submitted herewith on a separate sheet:

A method of fabricating complementary high-voltage field-effect transistors in a substrate of a first conductivity type includes forming first and second well regions of a second conductivity type in the substrate. A first drain region of the second conductivity type is formed in the first well region, and a first source region is formed in the substrate adjacent the first well region. Second and third drain regions of the first conductivity type are formed in the second well region separated from one another. A second source region of the first conductivity type is formed in the second well region separated from the second drain region. First and second buried layers are formed within the first and second well regions, respectively, with the second buried layer connected to the second and third drain regions.

Paragraph [0001], amended as follows:

**[0001]** This application is a division of U.S. patent application no. 10/392,622 filed March 20, 2003, which is a continuation of U.S. patent application no. 10/292,744 filed November 12, 2002, which is a continuation of U.S. patent application no. 10/176,325, filed June 20, 2002, now U.S. Patent 6,504,209, which is a continuation of U.S. patent application no. 09/769,649, filed January 24, 2001, now U.S. Patent 6,424,007, each of which is assigned to the assignee of the

present application. This application is also related to U.S. patent application nos. 09/245,029, now U.S. Patent 6,168,983, which is herein incorporated by reference, 10/292,744, now U.S. Patent 6,563,171, 10/176,345, now U.S. Patent 6,501,130, and 10/175,557, now U.S. Patent 6,465,291, which applications are assigned to the assignee of the present application ~~and are herein incorporated by reference~~.

Paragraph [0016], amended as follows:

**[0016]** Channel region 31 is defined at one end by P+ source diffusion region 19 and at the other end by P-type diffusion region 16, which extends down from the substrate surface of N-well 12. A lateral high-voltage p-channel FET is formed by the series connection of the PMOS device and a P-type JFET transistor formed by high-energy implantation of a P-type dopant (e.g., boron) into N-well region 12. This high-energy implantation forms P-type buried layer 14, which is connected to ~~and~~ p-type diffusion region 16. Buried layer 14 comprises the conducting portion of the extended drain of the P-type JFET device. The charge in P-type buried region 14 is approximately $2 \times 10^{12}$ $cm^{-2}$ in this embodiment, resulting in an on-resistance that is about 50% lower ~~that~~ than traditional devices.

Paragraph [0028], amended as follows:

**[0028]** Thus, the spaced-apart P-type buried layer regions 14 in the HVFET of Figure 2 provide parallel conduction paths. By controlling the charge in each of the buried layer regions 14 the ability of the P-channel device to support high voltage ~~in~~ is not compromised. Moreover, in accordance with the above teachings, each additional conducting layer contributes an additional $2 \times 10^{12}$ $cm^{-2}$ of charge to further lower the on-resistance of the device.